AMENDMENTS TO THE CLAIMS:

The following listing of claims will replace any/all prior versions, and listings, of claims in the application, wherein additions are shown in underlined text and deletions are shown in strikethrough text.

1. (Currently Amended) A method for aligning a key in a semiconductor device, comprising the steps of:

preparing a semiconductor substrate that is divided into a scribe lane region and a main chip region;

depositing an oxide film on the semiconductor substrate ~~for forming an align key~~;

forming an area key and a first align key at the same time on the scribe lane region by selectively etching the oxide film ~~by using~~ with a N-well ion implantation mask;

performing ~~an~~ a N-well ion implantation on the region from which the oxide film is removed ~~from~~; and

forming a second align key in the area key after the N-well ion implantation step~~, whose formation is already finished by removing the oxide film, by a silicon etching method using~~ by using a semiconductor substrate etching step, wherein the semiconductor substrate etching step comprises selectively etching the semiconductor substrate using a P-well ion implantation mask, ~~upon a N-well process using~~ and a P-well ion implantation ~~mask~~ in a P-well ion implantation region;

wherein the area key surface and the first alignment key surface are distinctly segregated by intervening portions of the oxide layer.

2. (Currently Amended) The method of claim 1, ~~wherein~~ comprising dual etching the oxide film and the ~~silicon~~ semiconductor substrate ~~are dual etched~~ in the ~~silicon etching step~~ semiconductor substrate etching step.

3. (Currently Amended) The method of claim 1, ~~wherein~~ comprising depositing the oxide film ~~is deposited~~ at a thickness of 800Å to 1500Å ~~upon the N-well formation process~~.

4. (Currently Amended) The method of claim 1, wherein the method further comprises the step of removing ~~the photoresist used as~~ the N-well ion implantation mask before the N-well ion implantation step.

5. (Currently Amended) The method of claim 1, wherein the method further comprises the step of removing ~~the photoresist used as~~ the P-well ion implantation mask before the P-well ion implantation step.

6. (Currently Amended) The method of claim 1, wherein~~, upon performing an N-well selective etching process on the main chip region, the area key and~~ the first align key ~~using~~ is bounded by a step portion of the oxide film ~~are formed at the same time by selectively etching the scribe lane region~~.

7. (Currently Amended) The method of claim 1, wherein the area key ~~formed by N-well photo and selective etching processes~~ has a ~~size~~ width of 40μm to 90μm ~~in a forward directional shape, and the oxide film on a second align key forming region of the scribe lane is removed~~.

8. (Currently Amended) The method of claim 1, further comprising the step of aligning the semiconductor substrate using the first align key before forming the second align key. ~~wherein the semiconductor substrate is aligned using the first align key formed on the scribe lane upon the P-well photo process, and the second align key is formed in the area key where the oxide film is removed using the N-well photo process upon selective etching of the oxide film using a P-well ion implantation photo process.~~

9. (Currently Amended) The method of claim 1, ~~wherein, upon the P-well photo process,~~ comprising accurately aligning the second align key ~~to be formed on the scribe lane region is accurately aligned~~ in the area key ~~which the oxide film is removed~~ by ~~the alignment of~~ aligning with the first align key during the semiconductor substrate etching step.

10. (Currently Amended) The method of claim 9, wherein the semiconductor substrate etching step further comprises simultaneously etching the oxide film in the P-well ion implantation region with the selective etching of the semiconductor substrate. ~~a silicon etching using the second align key as a pattern is performed using the oxide film removal process for the P-well ion implantation, simultaneously with the oxide film etching.~~

11. (Currently Amended) The method of claim 9, wherein ~~the silicon of the second align key patterning portion is etched at a thickness of 800 to 1500Å by performing a silicon etching for the formation of the second align key at~~ the semiconductor substrate etching step has an etching selection ratio of 0.8 to 1.2 and the resulting depth of the second align key is 800Å to 1500Å.

12. (Currently Amended) The method of claim 9, wherein the second align key ~~formed on the scribe lane region upon the P-well process~~ has the same shape as the first align key~~, thereby enabling a mask alignment using the second align key upon the subsequent photo process such as LOCOS, etc~~.